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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,838	11/26/2003	Suan Jeung Boon	303.601US3	8165
21186 7590 01/09/2008 SCHWEGMAN, LUNDBERG & WOESSNER, P.A. P.O. BOX 2938			EXAMINER	
			MITCHELL, JAMES M	
MINNEAPOLIS, MN 55402		ART UNIT	PAPER NUMBER	
			2813	·
		MAIL DATE	DELIVERY MODE	
			01/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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	Application No.	Applicant(s)			
	10/722,838	BOON, SUAN JEUNG			
Office Action Summary	Examiner	Art Unit			
	James M. Mitchell	2813			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPL WHICHEVER IS LONGER, FROM THE MAILING D. - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period. - Failure to reply within the set or extended period for reply will, by statut Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNIC 136(a). In no event, however, may a re will apply and will expire SIX (6) MONT te, cause the application to become ABA	ATION. ply be timely filed "HS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed on 05 J	<u>luly 2007</u> .				
2a)⊠ This action is FINAL 2b)□ Thi	This action is FINAL . 2b) ☐ This action is non-final.				
· · · · · · · · · · · · · · · · · · ·	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is				
closed in accordance with the practice under	Ex parte Quayle, 1935 C.D.	11, 453 O.G. 213.			
Disposition of Claims					
4) ⊠ Claim(s) 1-9,27-33 and 59-66 is/are pending in 4a) Of the above claim(s) is/are withdrates 5) □ Claim(s) is/are allowed. 6) ⊠ Claim(s) 1-9,27-33 and 59-66 is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and/or	awn from consideration.				
Application Papers					
9) The specification is objected to by the Examina 10) The drawing(s) filed on is/are: a) accomposed and applicant may not request that any objection to the Replacement drawing sheet(s) including the correct of the oath or declaration is objected to by the Examination.	cepted or b) objected to be drawing(s) be held in abeyand ction is required if the drawing(s)	ce. See 37 CFR 1.85(a). s) is objected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08)	Paper No(s)	ummary (PTO-413) /Mail Date formal Patent Application			
Paper No(s)/Mail Date 10 Information Disclosure Statement(s) (PTO/SB/08) 11 Information Disclosure Statement(s) (PTO/SB/08) 12 Information Disclosure Statement(s) (PTO/SB/08) 13 Information Disclosure Statement(s) (PTO/SB/08) 14 Information Disclosure Statement(s) (PTO/SB/08) 15 Information Disclosure Statement(s) (PTO/SB/08) 16 Information Disclosure Statement(s) (PTO/SB/08) 17 Information Disclosure Statement(s) (PTO/SB/08) 18 Information Disclosure Statement(s) (PTO/SB/08) 19 Information Disclosure Statement(s) (PTO/SB/08) 10 Information Disclosure Statement(s) (PTO/SB/08) 10 Information Disclosure Statement(s) (PTO/SB/08) 11 Information Disclosure Statement(s) (PTO/SB/08) 12 Information Disclosure Statement(s) (PTO/SB/08) 13 Information Disclosure Statement(s) (PTO/SB/08) 14 Information Disclosure Statement(s) (PTO/SB/08) 15 Information Disclosure Statement(s) (PTO/SB/08) 16 Information Disclosure Statement(s) (PTO/SB/08) 17 Information Disclosure Statement(s) (PTO/SB/08) 18 Information Disclosure Statement(s) (PTO/SB/08) 19 Information Disclosure Statement(s) (PTO/SB/08) 10 Information Disclosure Statement(s) (

DETAILED ACTION

This office action is in response to applicant's amendment filed July 5,
 2007.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35
 U.S.C. 102 that form the basis for the rejections under this section made in this
 Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 3 Claims 27-31 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Chung (U.S. 6,399,178).
- (cl. 27) A method of packaging comprising: providing an adhesive layer (e.g. 12); after providing the adhesive layer, forming an array of conductive elements within (Fig. 2→Fig. 9) the adhesive layer; and after forming the array of conductive elements within the adhesive layer, applying the adhesive layer having the array of conductive elements within the adhesive layer to a first side of a finished wafer (Fig. 9→Fig. 10), the first side of the finished wafer (Col. 11, Lines 45-47) having one or more dice to couple the array of conductive elements electrically to an array of connection pads (32) on a first die of the one or more dice;

(cl. 28) wherein forming an array of conductive elements within the adhesive

layer includes forming openings (e.g. 14; Fig. 2) in the adhesive layer and forming conductive material in the openings to form the array of conductive elements (Col. 14, Lines 27-41);

- (cl. 29) forming openings in the adhesive layer includes forming openings by laser cutting, chemical etching, or die cutting (Col.17, Lines 55-56);
- (cl. 30, 31) wherein forming an array of conductive elements includes forming an array of solder columns or balls/ bump (Col.15, Lines 43-45);
- (cl. 33) singulating the first die from the finished wafer and forming an individual flip chip package (Col. 11, Line 50).

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung (U.S. 6,399,178) in combination with Yoshizawa (U.S. 5,819,406).
- 6. Chung discloses the elements stated in paragraph 3 of this office action, but does not appear to show applying to its adhesive layer a film with a removable backing and removing the removable backing after securing the adhesive lager to the first side of a finished wafer.
- 7. Yoshizawa utilizes a removable backing applied to its adhesive and removing the removable backing layer (Fig. 24A→24F).

- 8. It would have been obvious to one of ordinary skill in the art to incorporate with the adhesive of Chung a removable backing in order to fill holes within its adhesive as taught by Yoshizawa (Fig. 24D→24E).
- 9. With respect to the removable layer being taken off after attaching the adhesive to the wafer, applicant has not disclosed that the claimed sequence is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. As such, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, the sequence would have been obvious, since it has been held that well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).
- 10. Claims 1-4, 6-9, 59, 60 and 62-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delfice et. al. al. (U.S. 6,190,940) in combination with Gilleo et al. (U.S. 6,228,678).and Nguyen'595 (U.S. (U.S. 6,245,595).
- 11. Delfice (Fig. 5-8) discloses:
- (cl. 1, 59) a method of packaging comprising: applying an adhesive (23) to a first side of a semiconductor (e.g. top of 21; Fig. 4), the first side of the finished having at least one die; after applying the adhesive (e.g. epoxy") to the first (e.g.

top surface, 21; Fig. 4)) and forming an array of conductive elements (35) within the adhesive to a level substantially flush with a surface of the adhesive (Fig. 5), the surface being a distal to the first side (Fig. 8) to allow the adhesive to contact a support (37) at initial contact of the array of conductive elements with the support, the array of conductive elements electrically coupled to an array of connection pads (22) on the at least one die; wherein the array of conductive elements (35) includes a plurality of conductive elements (35);

- (cl. 2, 3, cont. 59, 60) forming the array includes creating openings in the adhesive (Fig. 4), the openings (31) aligned with an array of connection pads (22) and substantially filling the openings (Fig. 5) with a conductive paste (Col. 5, Lines 35-37);
- (cl. 6) forming flip chip (Fig. 8);
- (cl. 7) surface mounting the flip chip package to a receiving support (Fig. 8);
- (cl. 8) curing adhesive (Abstract).
- (cl. 9) wherein forming conductive elements is selected from conductive paste (Col. 5, Lines 35-37);
- (cl. 60) e.g. paste in holes and therefore use of a dispensing apparatus;
- (cl. 62) the adhesive is cured (25; Fig. 3) prior to filling the array (Fig. 5);
- (cl. 64) coupling an individual die to a substrate providing interface with external circuitry and therefore a motherboard (Fig. 8; Col. 3, Lines 49-52).
- 12. Delfice does not appear to disclose singulating an adhesive formed on a wafer or that its adhesive is one or more of an elastomer material.

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However Gilleo teaches packaging chips at the wafer level and singulation
 (Col. 46-49).

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- 14. It would haven obvious to one of ordinary skill in the art to form the adhesive/ underfill on a wafer and then singulating in order to provide a streamline packaging process to form flip chips as taught by Gilleo (Col. 2, Lines 31-34).
- 15. Nguyen'595 discloses applying an elastomer coating (e.g. silicon"; Col. 4, Lines 14-21) in liquid form ("inject"; step 610; Fig. 6).
- 16. It would have been obvious to one of ordinary skill in the art to modify the process of Delfice by incorporating an elastomer adhesive/underfill etc. and applying it in liquid form as taught by Nguyen in order to apply a coating on a surface as required by Delfice (Fig. 4) and to provide a reduction in thermal stress as taught by Nguyen'595 (Col. 4, Lines 45-61).
- 17. With respect to forming a chamfer around the opening¹, applicant has not disclosed that the bevel shape groove is for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. As such, the claimed limitation would have been obvious to one of ordinary skill in the art, since, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d

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1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

- 18. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Delfice et. al. al. (U.S. 6,190,940), Gilleo et al. (U.S. 6,228,678) and Nguyen'595 (U.S. 6,245,595) as applied to claim 4 and further in combination with Kim et al. (U.S. 6,903,451).
- 19. Neither Delfice, Gilleo or Nguyen'595 appears to show applying a protective coating to a second side of the wafer.
- 20. However, Kim (Fig. 24) utilizes applying a protective coating (82) to a second side (e.g., bottom) of the wafer.
- 21. It would have been obvious to one of ordinary skill in the art to incorporate applying a protective coating to a second side of the modified wafer including Delfice in order to protect wafer and eliminate defects as taught by Kim (Col. 6, Lines 25-35).
- 22. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Delfice et. al. al. (U.S. 6,190,940), Gilleo et al. (U.S. 6,228,678) and Nguyen'595 (U.S. 6,245,595) as applied to claim 59 and further in combination with Yamaji et al. (U.S. 6,159,837).

¹ Simply an opening with a bevel shape as shown in applicant's Figure 4.

- 23. Neither Delfice, Gilleo or Nguyen'595 appears to explicitly disclose applying stencil/screen printing techniques to place paste in openings.
- 24. However, Yamaji utilizes applying a stencil/screen printing techniques to place paste in openings (Col. 6, Lines 3-6).
- 25. It would have been obvious to one of ordinary skill in the art to incorporate a screen printing process to the openings of Nguen'881 in order to fill the openings with a conductive material as taught by Yamaji (Col. 6, Lines 3-6).

Response to Amendment

26. Applicant's arguments with respect to his amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ex. Mitchell December 26, 2007

THAO X. LE
PRIMARY PATENT EXAMINER